

Applicant : William F. Beausoleil, et al.
Appl. No. : 09/655,596
Examiner : Tuan A. Vu
Docket No. : 706316-1203

Listing of Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) In an emulation engine comprised of a plurality of modules, a work station external to the plurality of modules, and a maintenance bus for transferring data between the work station and said modules, each of said modules including a plurality of module processors and a module main memory unit accessible for data transfers during an emulation by each of said plurality of processors, each of said processors having a control store to store a programmable sequence of emulation steps that define logic states for its processor, a method to allow data transfers between said module main memory unit and said work station without interrupting an in progress emulation, comprising:

compiling said programmable sequence of emulation steps to include, in at least one step, a blocking code that is decoded, when the step is read from the control store, as a disable command between the plurality of module processors and said module main memory;

decoding said blocking code and, in response thereto, blocking transfers between the plurality of module processors and said module main memory; and

transferring external data between said work station and said module main memory while transfers between the plurality of module processors and said module main memory are blocked, wherein said blocking code blocks data transfers between said plurality of module processors and said module main memory during the emulation step that includes the blocking code thereby allowing external data to be transferred between said work station and said module main memory during the in progress emulation.

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2. (Previously Presented) A method to allow data transfers between said module main memory unit and said work station as in claim 1 further comprising unblocking transfers between the plurality of module processors and said module main memory when the decoding step is next in the sequence after said step that includes said blocking code.

3. (Original) A method to allow data transfers between said module main memory unit and said work station as in claim 1 wherein said programmable sequence is repeated and said decoding and transferring steps are repeated with each repetition of said programmable sequence.

4. (Original) A method to allow data transfers between said module main memory unit and said work station as in claim 2 wherein said programmable sequence is repeated and said decoding and transferring steps are repeated with each repetition of said programmable sequence.